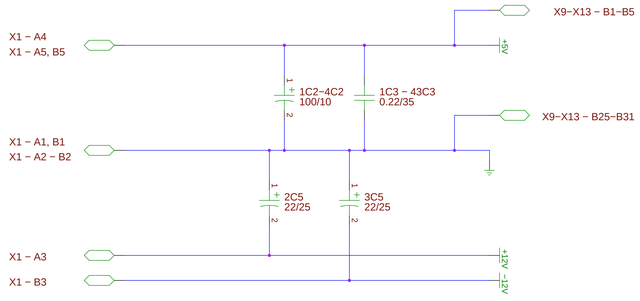
I.C. TYPE	+5V (PIN)	GND	+12V (PIN)	−12V (PIN)	DESIGNATIONS	SPARE GATES
B084	14	7	4	11	10,12,15	
B3170V			3		4,5	
D461D	14	7	8		7	
DL000D	14	7			34,62,121	34 − D
DL002D	14	7			25,33,83,108	
DL003D	14	7			40,42	40 − B,C
DL004D	14	7			8,22,30,64,103 120	8 − B,D , 103 − B , 120 − B,D
DL008D	14	7			32,65,93,102,116	102 − B , 116 − B
DL010D	14	7			17,27,47	
DL011D	14	7			23,63,94,99	23 − B , 63 − C
DL014D	14	7			48	48 − D
DL020D	14	7			24,28,109	109 − A
DL021D	14	7			85,92	
DL030D	14	7			100	
DL032D	14	7			79,101,108,117	
DL040D	14	7			80	
DL074D	14	7			57,78,81,91,95,96 118	96 − A
DL093D	14	7			119	
DL175D	16	8			115	
DL193D	16	8			49	
DL373D	20	10			38,43−45,51	
DL540D	20	10			18,69	
DL541D	20	10			37,41,46,50,53,54 56,84,90,97,98,114	

I.C. TYPE	+5V (PIN)	GND	+12V (PIN)	−12V (PIN)	DESIGNATIONS	SPARE GATES
DL8127D	24	12			36	
DS8205D	16	8			70,71,104,105,106	
DS8282	20	10			55,68,80	
DS8286	20	10			20,39,52,66,67	
K.170.UP.2	15	8			11,13,14	
K531SP1P	16	8			86,87	
MB111	7	6			6,9	
MH74S00	14	7			26	
MH74S04	14	7			35	
MH74S112	16	8			29	
MH74S51	14	7			16	
MH74S74	14	7			82	
U214D20	18	9			72−75	
U2732C45	24	12			58−61	
UA855D	26	11			19,110,111	
UA8560D	9	31			76,77	
UA857D	24	5			112,113	
UB8001C	11	36			21	
UB8010C	11	35			1−3	

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IKa, 1/4W, 5%
2. CAPACITOR VALUES ARE IN MICROFARADS.



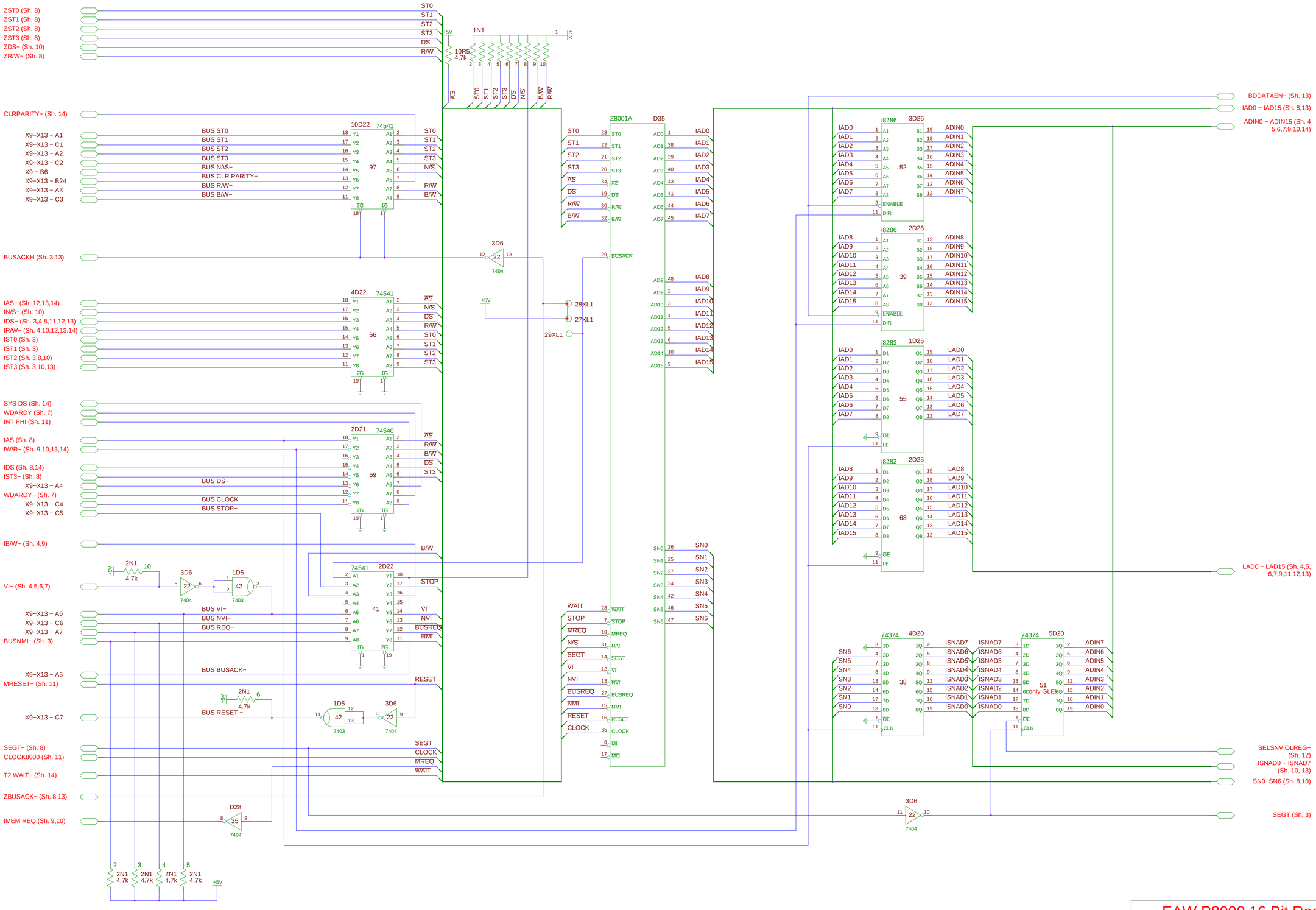
REF DESIGNATION	
LAST USED	NOT USED
C10	———
N1	———
U1	———
R12	———
D41	———

EAW P8000 16 Bit Rechner

TITLE

FILE: Stromlaufplan_01.sch | REVISION: 1.0

PAGE 1 OF 14 | DRAWN BY: Oliver Lehmann <lehmann@ans−netz.de>


ZST0 (Sh. 8)
ZST1 (Sh. 8)
ZST2 (Sh. 8)
ZST3 (Sh. 8)
ZDS~ (Sh. 10)
ZR/W~ (Sh. 8)
ST0
ST1
ST2
ST3
DS
R/W
+5V
1N1
10R5
4.7k
AS
B/W
N/S
CLRPARITY~ (Sh. 14)
X9~X13 ~ A1
X9~X13 ~ C1
X9~X13 ~ A2
X9~X13 ~ C2
X9 ~ B6
X9~X13 ~ B24
X9~X13 ~ A3
X9~X13 ~ C3
BUS ST0
BUS ST1
BUS ST2
BUS ST3
BUS N/S~
BUS CLR PARITY~
BUS R/W~
BUS B/W~
10D22
74541
97
2G
1G
BUSACKH (Sh. 3,13)
3D6
22
7404
Z8001A
D35
BUSACK
IAS~ (Sh. 12,13,14)
IN/S~ (Sh. 10)
IDS~ (Sh. 3,4,8,11,12,13)
IR/W~ (Sh. 4,10,12,13,14)
IST0 (Sh. 3)
IST1 (Sh. 3)
IST2 (Sh. 3,8,10)
IST3 (Sh. 3,10,13)
4D22
74541
56
28XL1
27XL1
29XL1
+5V
SYS DS (Sh. 14)
WDARDY (Sh. 7)
INT PHI (Sh. 11)
IAS (Sh. 8)
IW/R~ (Sh. 9,10,13,14)
IDS (Sh. 8,14)
IST3~ (Sh. 8)
X9~X13 ~ A4
WDARDY~ (Sh. 7)
X9~X13 ~ C4
X9~X13 ~ C5
2D21
74540
69
BUS DS~
BUS CLOCK
BUS STOP~
IB/W~ (Sh. 4,9)
VI~ (Sh. 4,5,6,7)
X9~X13 ~ A6
X9~X13 ~ C6
X9~X13 ~ A7
BUSNMI~ (Sh. 3)
2N1
10
4.7k
1D5
42
7403
BUS VI~
BUS NVI~
BUS REQ~
74541
2D22
41
X9~X13 ~ A5
MRESET~ (Sh. 11)
BUS BUSACK~
BUS RESET ~
X9~X13 ~ C7
SEGT~ (Sh. 8)
CLOCK8000 (Sh. 11)
T2 WAIT~ (Sh. 14)
ZBUSACK~ (Sh. 8,13)
IMEM REQ (Sh. 9,10)
D28
35
WAIT
STOP
MREQ
N/S
SEGT
VI
NVI
BUSREQ
NMI
RESET
CLOCK
MI
MO
SN0
SN1
SN2
SN3
SN4
SN5
SN6
BDDATAEN~ (Sh. 13)
IAD0 ~ IAD15 (Sh. 8,13)
ADIN0 ~ ADIN15 (Sh. 4
5,6,7,9,10,14)
i8286
3D26
52
IAD0
IAD1
IAD2
IAD3
IAD4
IAD5
IAD6
IAD7
ADIN0
ADIN1
ADIN2
ADIN3
ADIN4
ADIN5
ADIN6
ADIN7
ENABLE
DIR
2D26
39
IAD8
IAD9
IAD10
IAD11
IAD12
IAD13
IAD14
IAD15
ADIN8
ADIN9
ADIN10
ADIN11
ADIN12
ADIN13
ADIN14
ADIN15
i8282
1D25
55
LAD0
LAD1
LAD2
LAD3
LAD4
LAD5
LAD6
LAD7
OE
LE
2D25
68
LAD8
LAD9
LAD10
LAD11
LAD12
LAD13
LAD14
LAD15
LAD0 ~ LAD15 (Sh. 4,5,
6,7,9,11,12,13)
74374
4D20
38
ISNAD7
ISNAD6
ISNAD5
ISNAD4
ISNAD3
ISNAD2
ISNAD1
ISNAD0
CLK
5D20
51
only GLE1
ADIN7
ADIN6
ADIN5
ADIN4
ADIN3
ADIN2
ADIN1
ADIN0
SELSNVIOLREG~
(Sh. 12)
ISNAD0 ~ ISNAD7
(Sh. 10, 13)
SN0~SN6 (Sh. 8,10)
SEGT (Sh. 3)
Z8001A CPU
Segment Violation Register 5D20
EAW P8000 16 Bit Rechner
TITLE
FILE: Stromlaufplan_02.sch
REVISION: 1.1
PAGE 2 OF 14
DRAWN BY: Oliver Lehmann <lehmann@ans~netz.de>

IAD0 – IAD15 (Sh. 2)

ADIN0 – IADIN7 (Sh. 2)

74374 3D20 — 43

IAD0 IAD1 IAD2 IAD3 IAD4 IAD5 IAD6 IAD7

ADIN0 ADIN1 ADIN2 ADIN3 ADIN4 ADIN5 ADIN6 ADIN7

74374 1D20 — 45

ADIN0 ADIN1 ADIN2 ADIN3 ADIN4 ADIN5 ADIN6 ADIN7

IF1LOBYTE– (Sh. 12)

74374 2D20 — 44

IAD7 IAD6 IAD5 IAD4 IAD3 IAD2 IAD1 IAD0

ADIN7 ADIN6 ADIN5 ADIN4 ADIN3 ADIN2 ADIN1 ADIN0

TRPLOBYTE– (Sh. 12)

SEGT (Sh. 2)

7432 — 79 — 1D14

IST0 (Sh. 2)

IST1 (Sh. 2)

IST2 (Sh. 2)

IST3 (Sh. 2)

74138 2D24 — 70

I/O REF– (Sh. 11,12)

SEGTACK (Sh. 8)

VIACK– (Sh. 12)

MMU/EPUREF– (Sh. 11,13)

3D6 — 22 — 7404

2D12 — 85 — 7421

74138 1D24 — 71

STACKMEMREQ– (Sh. 4)

INSTFETCH1STWD– (Sh.8)

X3 – A2

3D3 — 121 — 7400

39XL1

38XL1

X3 – B2

3D3 — 121 — 7400

74541 9D22 — 98

BUS RFSN– X9–X13 – A9

BUS I/O– X9–X13 – C8

BUS MI– X9–X13 – C10

BUS AS– X9–X13 – A10

BUS MREQ– X9–X13 – C9

BUS RD– X9–X13 – C11

BUS IORQ– X9–X13 – A11

M1– (Sh. 12)

SYS AS– (Sh. 14)

IMEM REQ– (Sh. 10)

RD– (Sh. 12)

IORQ– (Sh. 12)

BUSACKH (Sh. 2)

X3 – B5

NMIU 8000–

18R5 — 4.7k — +5V

5D6 — 103 — 7404

MANUAL NMI (Sh. 10)

3D6 — 22 — 7404

BUS NMI (Sh. 2)

LATCHMEMERROR (Sh. 4)

3D8 — 47 — 7410

1D5 — 42 — 7403

BUS NMI–

X9 – B7

POWERFAIL– (Sh. 11)

2D3 — 62 — 7400

ONBDNMI– (Sh. 12)

1D14 — 79 — 7432

ENAONBDNMI– (Sh. 10)

IDS– (Sh. 2)

External Violation Registers
VIACK– generation

EAW P8000 16 Bit Rechner

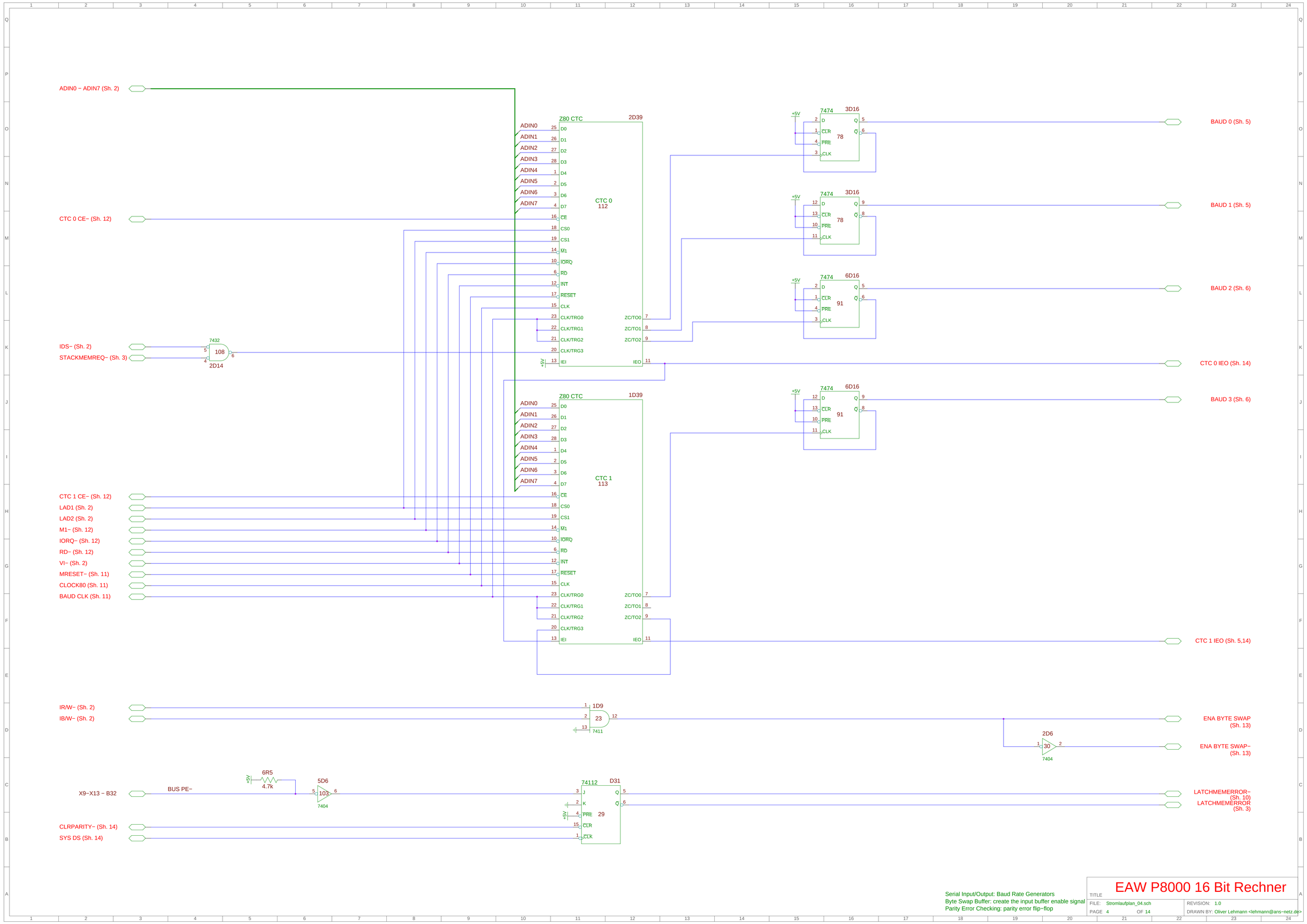
TITLE

FILE: Stromlaufplan_03.sch

REVISION: 1.0

PAGE 3 OF 14

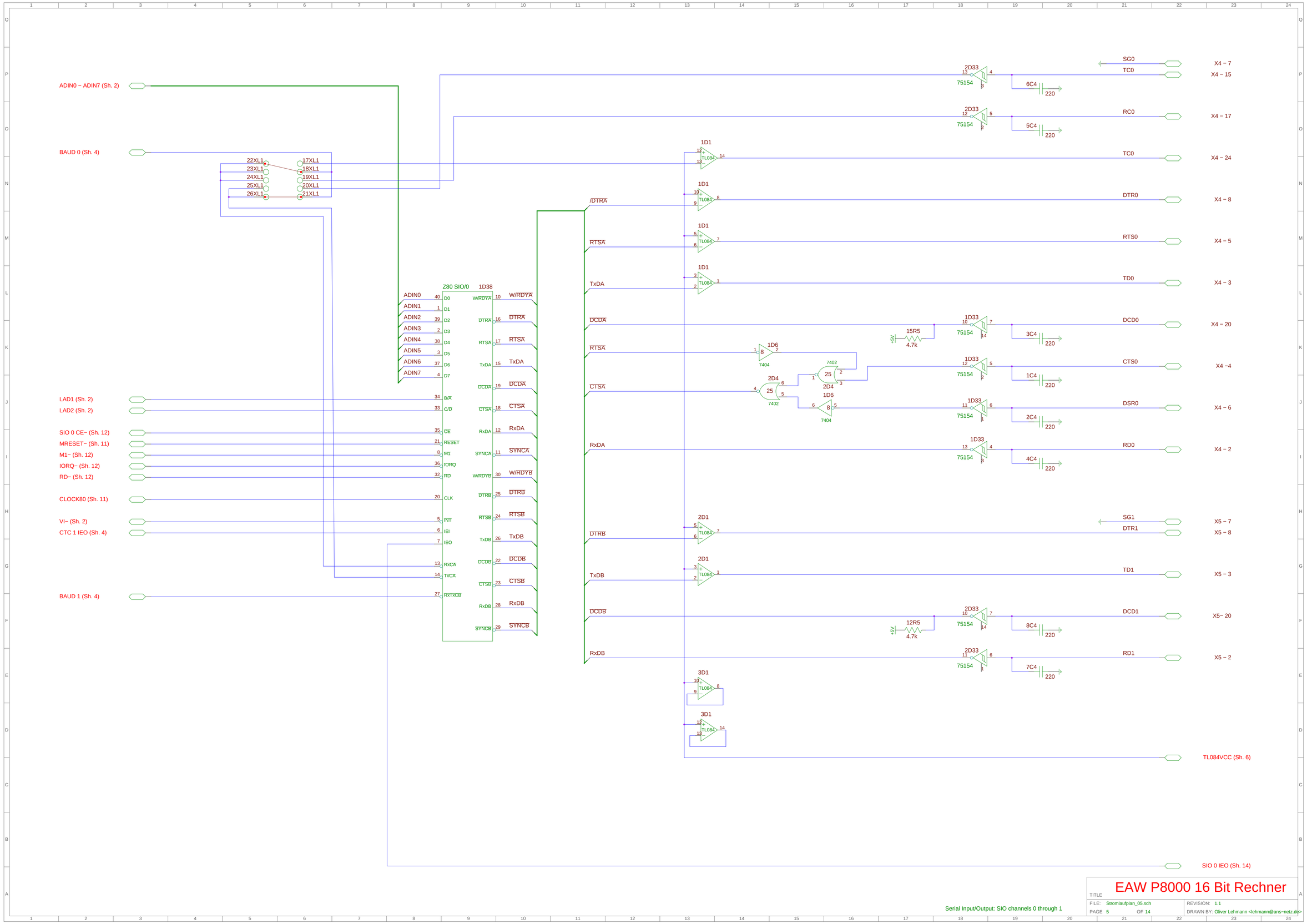
DRAWN BY: Oliver Lehmann <lehmann@ans-netz.de>



Serial Input/Output: Baud Rate Generators
Byte Swap Buffer: create the input buffer enable signal
Parity Error Checking: parity error flip–flop

EAW P8000 16 Bit Rechner

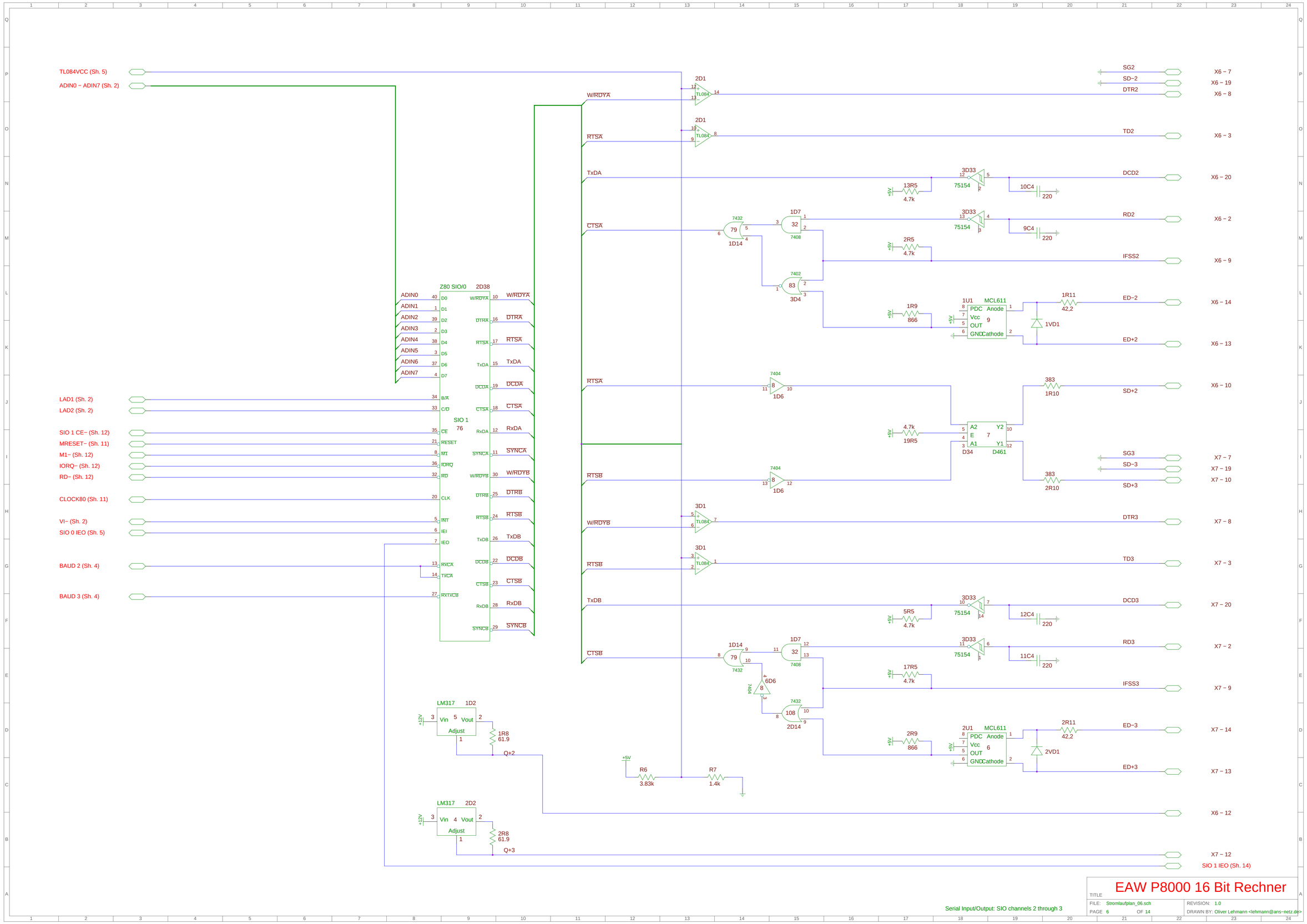
TITLE	
FILE: Stromlaufplan_04.sch	REVISION: 1.0
PAGE 4 OF 14	DRAWN BY: Oliver Lehmann <lehmann@ans-netz.de>



Serial Input/Output: SIO channels 0 through 1

EAW P8000 16 Bit Rechner

TITLE	
FILE: Stromlaufplan_05.sch	REVISION: 1.1
PAGE 5 OF 14	DRAWN BY: Oliver Lehmann <lehmann@ans-netz.de>



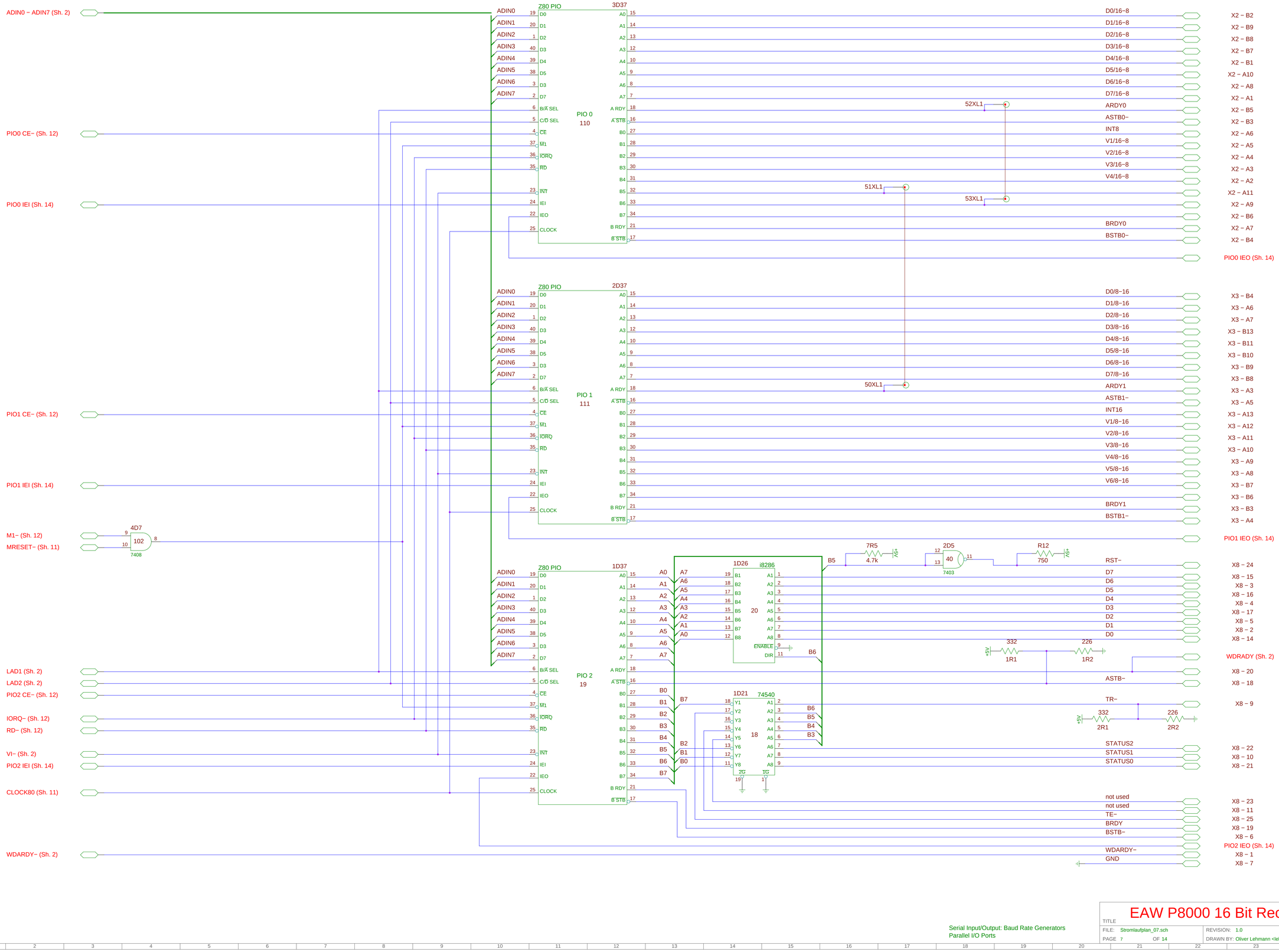
Serial Input/Output: SIO channels 2 through 3

EAW P8000 16 Bit Rechner

TITLE

FILE: Stromlaufplan_06.sch | REVISION: 1.0

PAGE 6 OF 14 | DRAWN BY: Oliver Lehmann <lehmann@ans-netz.de>


ADIN0 – ADIN7 (Sh. 2)
PIO0 CE– (Sh. 12)
PIO0 IEI (Sh. 14)
PIO1 CE– (Sh. 12)
PIO1 IEI (Sh. 14)
M1– (Sh. 12)
MRESET– (Sh. 11)
LAD1 (Sh. 2)
LAD2 (Sh. 2)
PIO2 CE– (Sh. 12)
IORQ– (Sh. 12)
RD– (Sh. 12)
VI– (Sh. 2)
PIO2 IEI (Sh. 14)
CLOCK80 (Sh. 11)
WDARDY– (Sh. 2)
4D7
102
7408
Z80 PIO
3D37
PIO 0
110
2D37
PIO 1
111
1D37
PIO 2
19
ADIN0
ADIN1
ADIN2
ADIN3
ADIN4
ADIN5
ADIN6
ADIN7
D0
D1
D2
D3
D4
D5
D3
D7
B/A SEL
C/D SEL
CE
M1
IORQ
RD
INT
IEI
IEO
CLOCK
A RDY
A STB
B RDY
B STB
A0
A1
A2
A3
A4
A5
A6
A7
B0
B1
B2
B3
B4
B5
B6
B7
52XL1
51XL1
53XL1
50XL1
D0/16–8
D1/16–8
D2/16–8
D3/16–8
D4/16–8
D5/16–8
D6/16–8
D7/16–8
ARDY0
ASTB0–
INT8
V1/16–8
V2/16–8
V3/16–8
V4/16–8
BRDY0
BSTB0–
PIO0 IEO (Sh. 14)
D0/8–16
D1/8–16
D2/8–16
D3/8–16
D4/8–16
D5/8–16
D6/8–16
D7/8–16
ARDY1
ASTB1–
INT16
V1/8–16
V2/8–16
V3/8–16
V4/8–16
V5/8–16
V6/8–16
BRDY1
BSTB1–
PIO1 IEO (Sh. 14)
1D26
i8286
20
ENABLE
DIR
1D21
74540
18
ZG
1G
7R5
4.7k
+5V
2D5
40
7403
R12
750
RST–
D7
D6
D5
D4
D3
D2
D1
D0
332
1R1
226
1R2
WDRADY (Sh. 2)
ASTB–
TR–
2R1
2R2
STATUS2
STATUS1
STATUS0
not used
not used
TE–
BRDY
BSTB–
WDARDY–
GND
X2 – B2
X2 – B9
X2 – B8
X2 – B7
X2 – B1
X2 – A10
X2 – A8
X2 – A1
X2 – B5
X2 – B3
X2 – A6
X2 – A5
X2 – A4
X2 – A3
X2 – A2
X2 – A11
X2 – A9
X2 – B6
X2 – A7
X2 – B4
X3 – B4
X3 – A6
X3 – A7
X3 – B13
X3 – B11
X3 – B10
X3 – B9
X3 – B8
X3 – A3
X3 – A5
X3 – A13
X3 – A12
X3 – A11
X3 – A10
X3 – A9
X3 – A8
X3 – B7
X3 – B6
X3 – B3
X3 – A4
PIO1 IEO (Sh. 14)
X8 – 24
X8 – 15
X8 – 3
X8 – 16
X8 – 4
X8 – 17
X8 – 5
X8 – 2
X8 – 14
X8 – 20
X8 – 18
X8 – 9
X8 – 22
X8 – 10
X8 – 21
X8 – 23
X8 – 11
X8 – 25
X8 – 19
X8 – 6
PIO2 IEO (Sh. 14)
X8 – 1
X8 – 7
Serial Input/Output: Baud Rate Generators
Parallel I/O Ports
EAW P8000 16 Bit Rechner
TITLE
FILE: Stromlaufplan_07.sch
REVISION: 1.0
PAGE 7 OF 14
DRAWN BY: Oliver Lehmann <lehmann@ans-netz.de>

IAD0 – IAD15 (Sh. 2)
SN0 – SN6 (Sh. 2)
ZST0 – ZST3 (Sh. 2)

Z8010 MMU 1D36 — STACK MMU 3
Z8010 MMU 2D36 — DATA MMU 2
Z8010 MMU 3D36 — CODE MMU 1

IAD8 40 AD8 — A8 22 TRAD8
IAD9 39 AD9 — A9 21 TRAD9
IAD10 38 AD10 — A10 20 TRAD10
IAD11 37 AD11 — A11 19 TRAD11
IAD12 34 AD12 — A12 18 TRAD12
IAD13 33 AD13 — A13 17 TRAD13
IAD14 32 AD14 — A14 16 TRAD14
IAD15 31 AD15 — A15 15 TRAD15
A16 14 TRAD16
SN0 30 SN0 — A17 13 TRAD17
SN1 29 SN1 — A18 12 TRAD18
SN2 28 SN2 — A19 10 TRAD19
SN3 27 SN3 — A20 9 TRAD20
SN4 26 SN4 — A21 8 TRAD21
SN5 25 SN5 — A22 7 TRAD22
SN6 24 SN6 — A23 6 TRAD23

ZST0 44 ST0 — SEGT 3
ZST1 43 ST1 — SUP 4
ZST2 42 ST2
ZST3 41 ST3
46 AS
45 DS
47 R/W
48 N/S
1 CS
5 RESET
36 CLK
2 DMASYNC

TRAD0 – TRAD23 (Sh. 13)
SEGT– (Sh. 2,3)
SUP– (Sh. 14)

4R5 4.7k +5V
9R5 4.7k +5V

ZBUSACK– (Sh. 2)
CLOCK8000 (Sh. 11)
MRESET– (Sh. 11)
ZR/W– (Sh.2)
IDS– (Sh. 2)

MSTACK– (Sh. 10)
LAD3 (Sh. 2)
MDATA– (Sh. 10)
LAD2 (Sh. 2)
MCODE– (Sh. 10)
LAD1 (Sh. 2)

IAS (Sh. 2)
PHI DELAY (Sh. 13)

7400 D27 26
74112 D31 — J K PRE CLR CLK Q
8R5 4.7k +5V
29
2D6 30 7404
D27 26 7400
1D7 32 7408
74112 2D31 — only GLE! 31
1D5 42 7403 — SEGT
7402 1D4 33
2D8 27 7410
74112 2D31 — only GLE! 31
2D5 40 7403 — SUP

AS PHI DELAY (Sh. 14)

INT 2 PHI (Sh. 11)
SEGTACK (Sh. 3)

SYS AS (Sh. 14)
INSTFETCH1STWD– (Sh. 3)
IDS (Sh. 2)
IST3– (Sh. 2)
IST2 (Sh. 2)

Memory Management Units

EAW P8000 16 Bit Rechner

TITLE	
FILE: Stromlaufplan_08.sch	REVISION: 1.0
PAGE 8 OF 14	DRAWN BY: Oliver Lehmann <lehmann@ans-netz.de>

ADIN0 − ADIN15 (Sh. 2)

LAD0 − LAD15 (Sh. 2)

2732 3D41 59
LAD1 8 A0 O0 9 ADIN0
LAD2 7 A1 O1 10 ADIN1
LAD3 6 A2 O2 11 ADIN2
LAD4 5 A3 O3 13 ADIN3
LAD5 4 A4 O4 14 ADIN4
LAD6 3 A5 O5 15 ADIN5
LAD7 2 A6 O6 16 ADIN6
LAD8 1 A7 O7 17 ADIN7
LAD9 23 A8
LAD10 22 A9
LAD11 19 A10
LAD12 21 A11
20 G/VPP
18 E

2732 4D41 58
LAD1 8 A0 O0 9 ADIN0
LAD2 7 A1 O1 10 ADIN1
LAD3 6 A2 O2 11 ADIN2
LAD4 5 A3 O3 13 ADIN3
LAD5 4 A4 O4 14 ADIN4
LAD6 3 A5 O5 15 ADIN5
LAD7 2 A6 O6 16 ADIN6
LAD8 1 A7 O7 17 ADIN7
LAD9 23 A8
LAD10 22 A9
LAD11 19 A10
LAD12 21 A11
20 G/VPP
18 E

2114 2D40 74
LAD1 5 A0 DQ1 14 ADIN8
LAD2 6 A1 DQ2 13 ADIN9
LAD3 7 A2 DQ3 12 ADIN10
LAD4 4 A3 DQ4 11 ADIN11
LAD5 3 A4
LAD6 2 A5
LAD7 1 A6
LAD8 17 A7
LAD9 16 A8
LAD10 15 A9
10 WE CS 8

2114 4D40 72
LAD1 5 A0 DQ1 14 ADIN0
LAD2 6 A1 DQ2 13 ADIN1
LAD3 7 A2 DQ3 12 ADIN2
LAD4 4 A3 DQ4 11 ADIN3
LAD5 3 A4
LAD6 2 A5
LAD7 1 A6
LAD8 17 A7
LAD9 16 A8
LAD10 15 A9
10 WE CS 8

2732 1D41 61
LAD1 8 A0 O0 9 ADIN8
LAD2 7 A1 O1 10 ADIN9
LAD3 6 A2 O2 11 ADIN10
LAD4 5 A3 O3 13 ADIN11
LAD5 4 A4 O4 14 ADIN12
LAD6 3 A5 O5 15 ADIN13
LAD7 2 A6 O6 16 ADIN14
LAD8 1 A7 O7 17 ADIN15
LAD9 23 A8
LAD10 22 A9
LAD11 19 A10
LAD12 21 A11
20 G/VPP
18 E

2732 2D41 60
LAD1 8 A0 O0 9 ADIN8
LAD2 7 A1 O1 10 ADIN9
LAD3 6 A2 O2 11 ADIN10
LAD4 5 A3 O3 13 ADIN11
LAD5 4 A4 O4 14 ADIN12
LAD6 3 A5 O5 15 ADIN13
LAD7 2 A6 O6 16 ADIN14
LAD8 1 A7 O7 17 ADIN15
LAD9 23 A8
LAD10 22 A9
LAD11 19 A10
LAD12 21 A11
20 G/VPP
18 E

2114 1D40 75
LAD1 5 A0 DQ1 14 ADIN12
LAD2 6 A1 DQ2 13 ADIN13
LAD3 7 A2 DQ3 12 ADIN14
LAD4 4 A3 DQ4 11 ADIN15
LAD5 3 A4
LAD6 2 A5
LAD7 1 A6
LAD8 17 A7
LAD9 16 A8
LAD10 15 A9
10 WE CS 8

2114 3D40 73
LAD1 5 A0 DQ1 14 ADIN4
LAD2 6 A1 DQ2 13 ADIN5
LAD3 7 A2 DQ3 12 ADIN6
LAD4 4 A3 DQ4 11 ADIN7
LAD5 3 A4
LAD6 2 A5
LAD7 1 A6
LAD8 17 A7
LAD9 16 A8
LAD10 15 A9
10 WE CS 8

BDMEMA2K− (Sh. 10)

IW/R− (Sh. 2)

BDMEMB2K− (Sh. 10)

3D14 7432
4 5 101 6
10 9 101 8

IMEM REQ (Sh. 2)

IW/R− (Sh. 2)

1D3 7400
9 10 34 8

LAD0 (Sh. 2)

5D6 7404
9 103 8

4D9 7411
3 4 5 99 6
9 10 11 99 8

3D14 7432
1 2 101 3
13 12 101 11

MEMC2KLO−

MEMC2KHI−

IB/W− (Sh. 2)

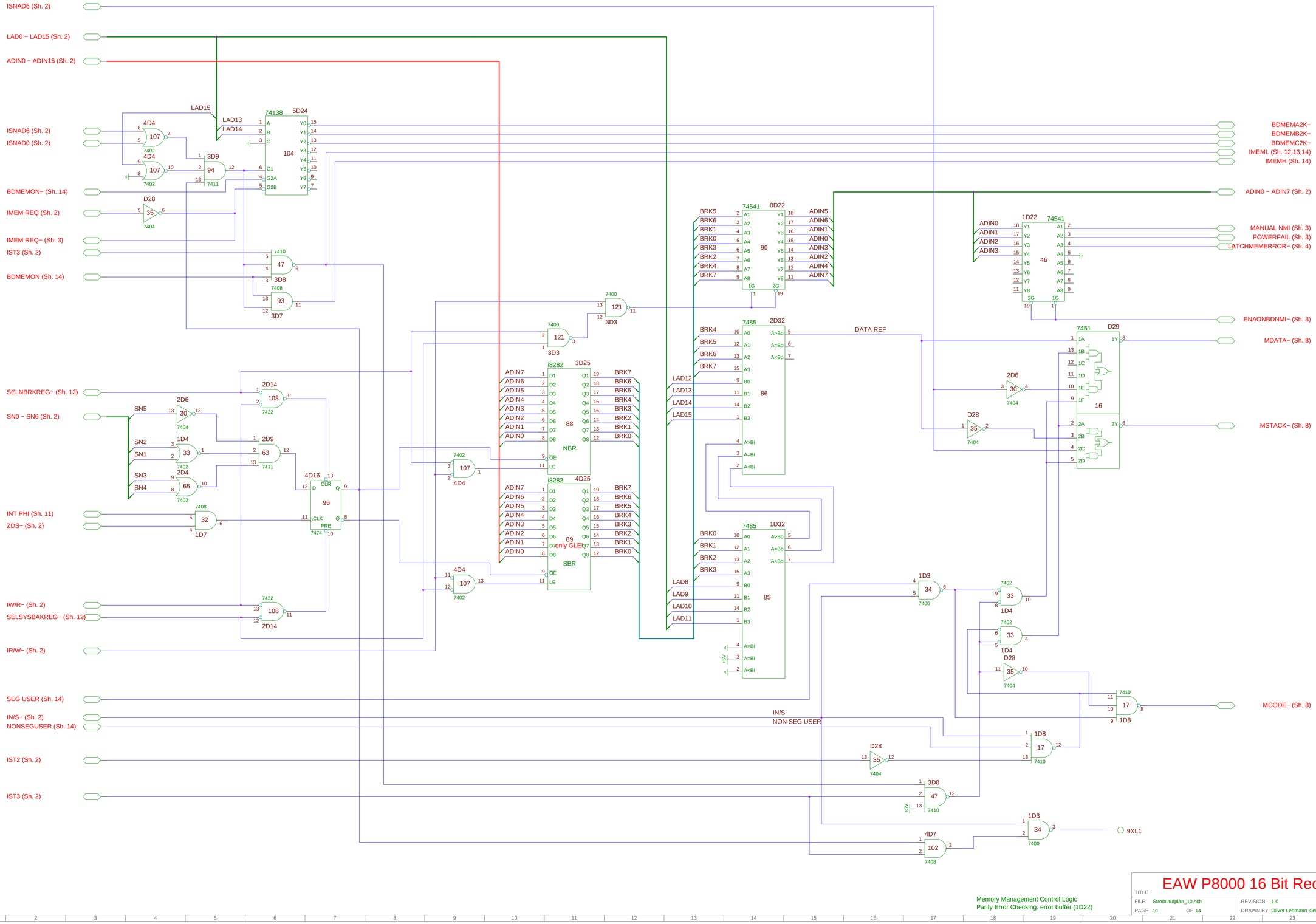
BDMEMC2K− (Sh. 10)

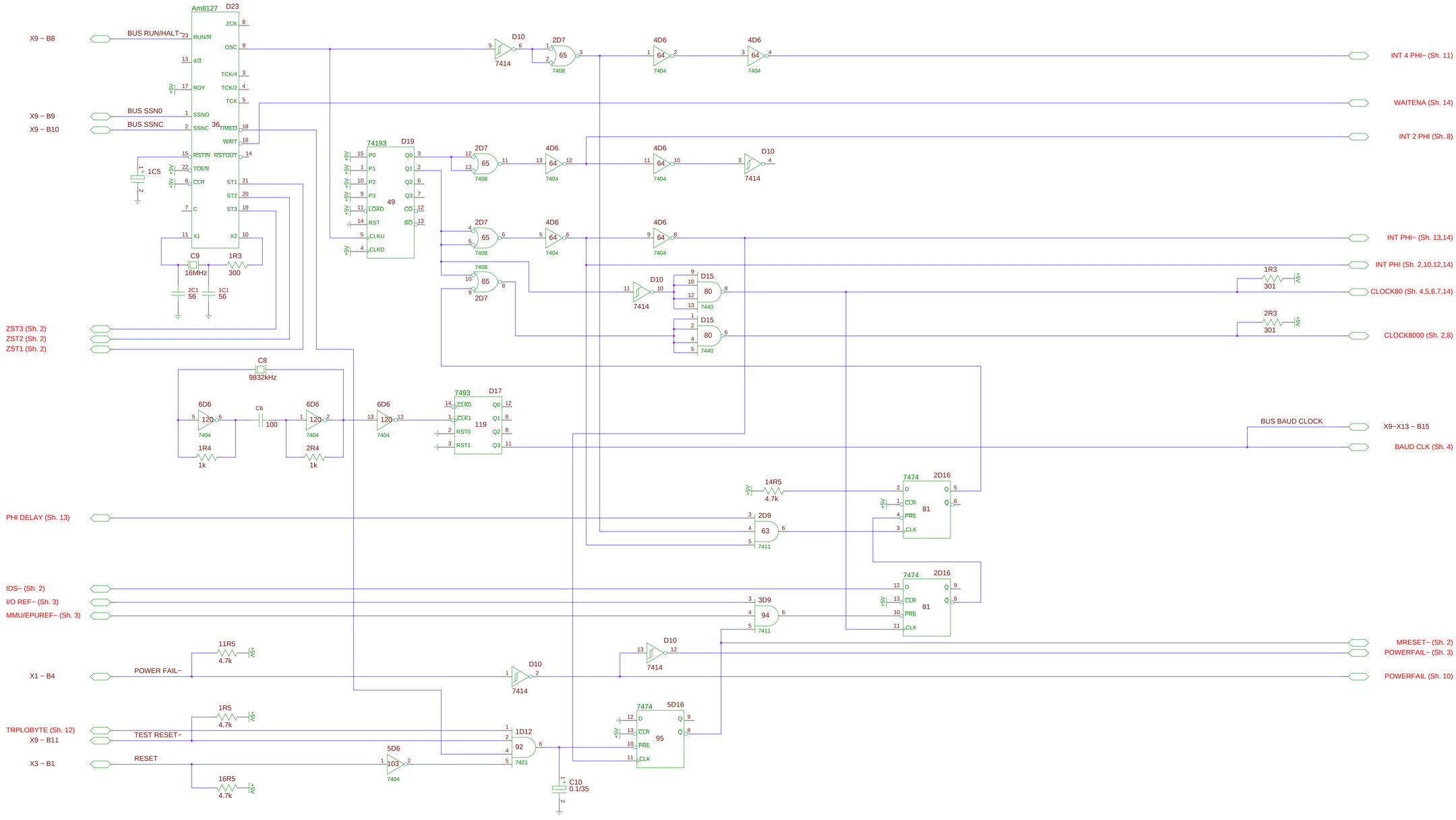
Read−Only Memory
Read/Write Memory

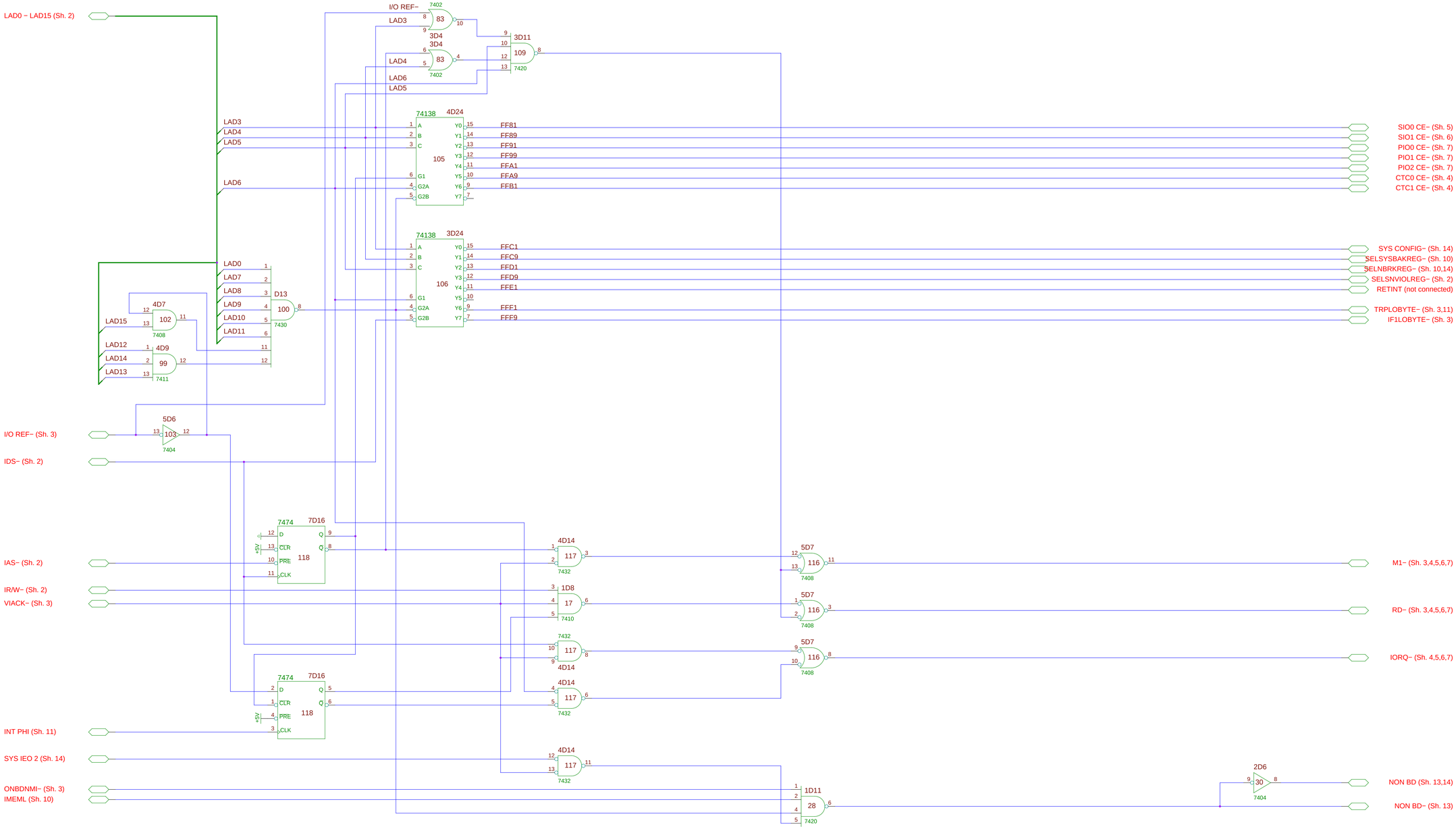
EAW P8000 16 Bit Rechner

TITLE

FILE: Stromlaufplan_09.sch
REVISION: 1.0
PAGE 9 OF 14
DRAWN BY: Oliver Lehmann <lehmann@ans−netz.de>


ISNAD6 (Sh. 2)
LAD0 – LAD15 (Sh. 2)
ADIN0 – ADIN15 (Sh. 2)
ISNAD6 (Sh. 2)
ISNAD0 (Sh. 2)
BDMEMON– (Sh. 14)
IMEM REQ (Sh. 2)
IMEM REQ– (Sh. 3)
IST3 (Sh. 2)
BDMEMON (Sh. 14)
SELNBRKREG– (Sh. 12)
SN0 – SN6 (Sh. 2)
INT PHI (Sh. 11)
ZDS– (Sh. 2)
IW/R– (Sh. 2)
SELSYSBAKREG– (Sh. 12)
IR/W– (Sh. 2)
SEG USER (Sh. 14)
IN/S– (Sh. 2)
NONSEGUSER (Sh. 14)
IST2 (Sh. 2)
IST3 (Sh. 2)
BDMEMA2K–
BDMEMB2K–
BDMEMC2K–
IMEML (Sh. 12,13,14)
IMEMH (Sh. 14)
ADIN0 – ADIN7 (Sh. 2)
MANUAL NMI (Sh. 3)
POWERFAIL (Sh. 3)
LATCHMEMERROR– (Sh. 4)
ENAONBDNMI– (Sh. 3)
MDATA– (Sh. 8)
MSTACK– (Sh. 8)
MCODE– (Sh. 8)
9XL1
DATA REF
IN/S
NON SEG USER
Memory Management Control Logic
Parity Error Checking: error buffer (1D22)
EAW P8000 16 Bit Rechner
TITLE
FILE: Stromlaufplan_10.sch
REVISION: 1.0
PAGE 10 OF 14
DRAWN BY: Oliver Lehmann <lehmann@ans-netz.de>


Am8127
D23
X9 − B8
BUS RUN/HALT
BUS SSN0
X9 − B9
BUS SSNC
X9 − B10
1C5
C9
16MHz
1R3
300
2C1
56
1C1
56
ZST3 (Sh. 2)
ZST2 (Sh. 2)
ZST1 (Sh. 2)
C8
9832kHz
6D6
C6
100
1R4
1k
2R4
1k
7493
D17
119
PHI DELAY (Sh. 13)
74193
D19
49
D10
7414
2D7
7408
4D6
7404
INT 4 PHI− (Sh. 11)
WAITENA (Sh. 14)
INT 2 PHI (Sh. 8)
INT PHI− (Sh. 13,14)
INT PHI (Sh. 2,10,12,14)
D15
7440
CLOCK80 (Sh. 4,5,6,7,14)
CLOCK8000 (Sh. 2,8)
BUS BAUD CLOCK
X9−X13 − B15
BAUD CLK (Sh. 4)
14R5
4.7k
7474
2D16
81
2D9
7411
IDS− (Sh. 2)
I/O REF− (Sh. 3)
MMU/EPUREF− (Sh. 3)
3D9
94
MRESET− (Sh. 2)
POWERFAIL− (Sh. 3)
POWERFAIL (Sh. 10)
11R5
X1 − B4
POWER FAIL−
1R5
TRPLOBYTE (Sh. 12)
X9 − B11
TEST RESET−
1D12
92
7421
X3 − B1
RESET
16R5
5D6
103
C10
0.1/35
5D16
95
Clock Generation Circuit (D19)
Baud Clock Generator (D17)
System Reset Logic (5D16)
T3 Wait State Generator Logic (2D16)
EAW P8000 16 Bit Rechner
TITLE
FILE: Stromlaufplan_11.sch
REVISION: 1.0
PAGE 11 OF 14
DRAWN BY: Oliver Lehmann <lehmann@ans-netz.de>



Peripheral Handshaking Logic (3D20, 4D20)

EAW P8000 16 Bit Rechner

TITLE

FILE: Stromlaufplan_12.sch | REVISION: 1.0

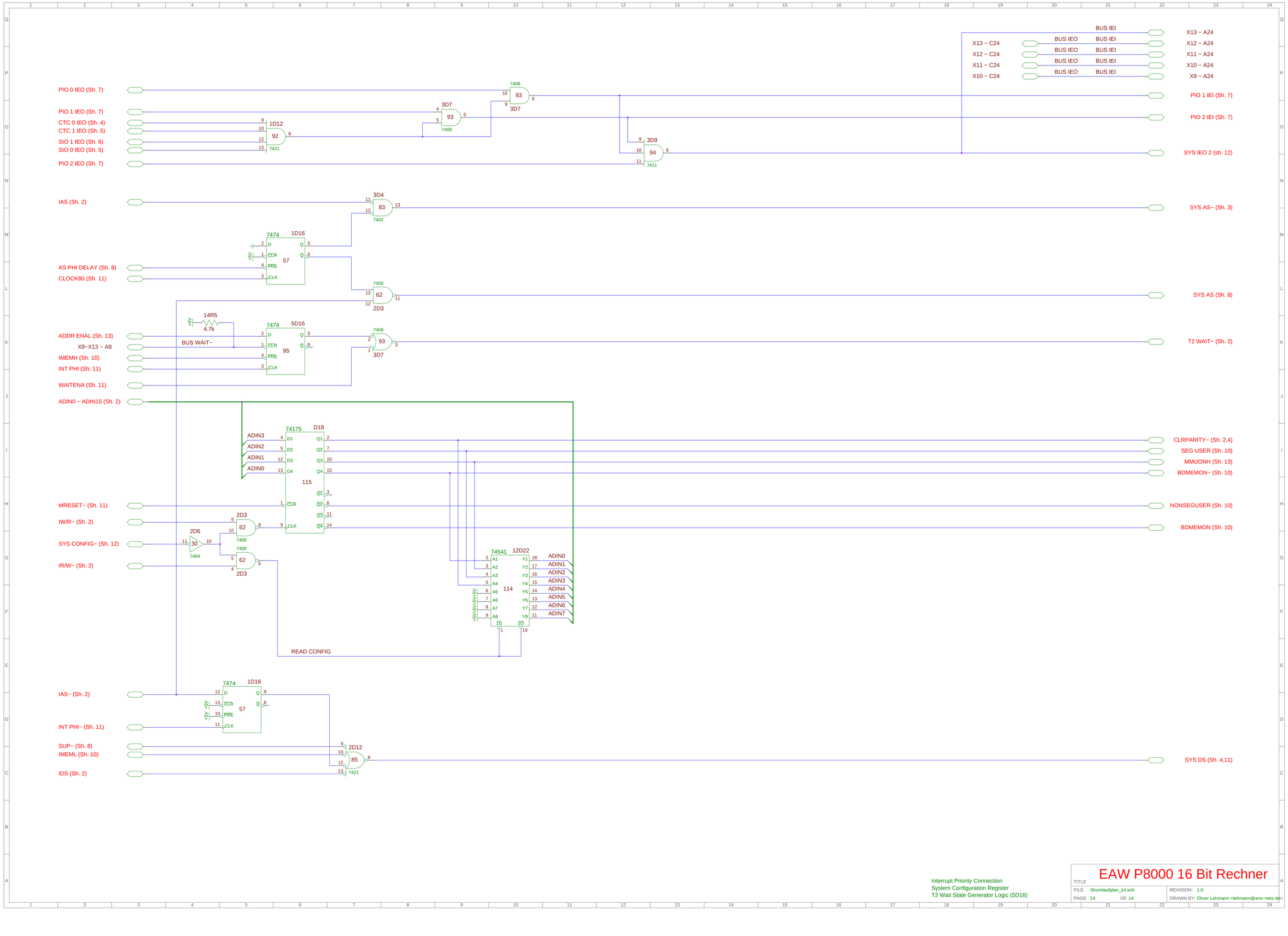
PAGE 12 OF 14 | DRAWN BY: Oliver Lehmann <lehmann@ans-netz.de>

INT PHI− (Sh. 11)
INT 4 PHI− (Sh. 11)
IAS− (Sh. 2)
NON BD− (Sh. 12)
NON BD (Sh. 12)
ENA BYTE SWAP− (Sh. 4)
ENA BYTE SWAP (Sh. 4)
IR/W− (Sh. 2)
MMU/EPUREF− (Sh. 3)
X9 − C24
ZBUSACK− (Sh. 2)
IW/R− (Sh. 2)
IDS− (Sh. 2)
MMUONH (Sh. 14)
IST3 (Sh. 2)
BUSACKH (Sh. 2)
IAD0 − IAD15 (Sh. 2)
LAD0 − LAD15 (Sh. 2)
ISNAD0 − ISNAD6 (Sh. 2)
TRAD0 − TRAD23 (Sh. 8)
TESTDATA−
PHI DELAY (Sh. 8,11)
ADDR ENAL (Sh. 14)
BD DATAEN− (Sh. 2)
7474 D30
82
2N1 7 4.7k
D27 26 7400
1D9 23 7411
2D4 25 7402
2D8 27 7410
1D11 28 7420
2D8 27 7410
2D11 24 7420
2D11 24 7420
D28 35 7404
D27 26 7400
6D22 53
3D22 37
7D22 50
11D22 84
5D22 54
5D26 66
4D26 67
i8286
Einsatz des Byte Swap Buffers (74541) vorgesehen aber nicht bestueckt. Wuerde bei aktiv AD0−7 auf IAD8−15 schalten
X9−X13 − C32 … C12
X9−X13 − A32 … A12
X9−X13 − A29 … A25
X9−X13 − C29 … C23
X9−X13 − A23 … A20
X9−X13 − C19 … C16
X9−X13 − A19 … A16
X9−X13 − C15 … A12

Address/Data Buffers and Steering Logic

EAW P8000 16 Bit Rechner

TITLE
FILE: Stromlaufplan_13.sch
REVISION: 1.0
PAGE 13 OF 14
DRAWN BY: Oliver Lehmann <lehmann@ans-netz.de>


BUS IEI
X13 – A24
X12 – A24
X11 – A24
X10 – A24
X9 – A24
X13 – C24
X12 – C24
X11 – C24
X10 – C24
BUS IEO
BUS IEI
PIO 0 IEO (Sh. 7)
PIO 1 IEO (Sh. 7)
CTC 0 IEO (Sh. 4)
CTC 1 IEO (Sh. 5)
SIO 1 IEO (Sh. 6)
SIO 0 IEO (Sh. 5)
PIO 2 IEO (Sh. 7)
7408
93
3D7
1D12
92
7421
7411
3D9
94
PIO 1 IEI (Sh. 7)
PIO 2 IEI (Sh. 7)
SYS IEO 2 (sh. 12)
IAS (Sh. 2)
3D4
83
7402
SYS AS– (Sh. 3)
7474
1D16
57
AS PHI DELAY (Sh. 8)
CLOCK80 (Sh. 11)
D
CLR
PRE
CLK
Q
7400
62
2D3
SYS AS (Sh. 8)
+5V
14R5
4.7k
5D16
95
ADDR ENAL (Sh. 13)
X9–X13 – A8
BUS WAIT–
IMEMH (Sh. 10)
INT PHI (Sh. 11)
T2 WAIT– (Sh. 2)
WAITENA (Sh. 11)
ADIN0 – ADIN15 (Sh. 2)
74175
D18
115
ADIN3
ADIN2
ADIN1
ADIN0
D1
D2
D3
D4
Q1
Q2
Q3
Q4
CLRPARITY– (Sh. 2,4)
SEG USER (Sh. 10)
MMUONH (Sh. 13)
BDMEMON– (Sh. 10)
MRESET– (Sh. 11)
IW/R– (Sh. 2)
SYS CONFIG– (Sh. 12)
IR/W– (Sh. 2)
2D6
30
7404
NONSEGUSER (Sh. 10)
BDMEMON (Sh. 10)
74541
12D22
114
ADIN4
ADIN5
ADIN6
ADIN7
READ CONFIG
IAS– (Sh. 2)
INT PHI– (Sh. 11)
SUP– (Sh. 8)
IMEML (Sh. 10)
IDS (Sh. 2)
2D12
85
SYS DS (Sh. 4,11)
Interrupt Priority Connection
System Configuration Register
T2 Wait State Generator Logic (5D16)
EAW P8000 16 Bit Rechner
TITLE
FILE: Stromlaufplan_14.sch
REVISION: 1.0
PAGE 14 OF 14
DRAWN BY: Oliver Lehmann <lehmann@ans-netz.de>